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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/849,126	05/04/2001	Avraham Mualem	042390.P10990	9064

7590 02/01/2007

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EXAMINER	
DINH, MINH	
ART UNIT	PAPER NUMBER
2132	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/849,126	MUALEM ET AL.	
	Examiner	Art Unit	
	Minh Dinh	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-26,28-31,33-36,38-41 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-26,28-31,33-36,38-41 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/27/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is in response to the amendment filed 11/20/06. Claims 24, 29, 34 and 38 have been amended; claims 27, 32, 37 and 42 have been canceled.

Response to Arguments

2. Applicant's arguments filed 11/20/06 have been fully considered but they are not persuasive. Applicant argues that one of ordinary skill in the art would not have been motivated to apply the teachings of Yoshida (5,928,372) to Anand (6,370,599) to produce the claimed invention because the teachings of Yoshida are limited to verifying data transferred between a data processor and an external recording unit (e.g., a disk drive using an ATA interface) and nothing in Yoshida suggest the desirability of using these data verification techniques to verify security association (SA) transferred between a data processor and a network adapter card (NIC) (page 7, last paragraph). Yoshida teaches a method for verifying data transferred between a data processor and a hard drive, which is a peripheral device, to prevent data transfer errors (col. 1, line 60 – col. 2, line 20; figures 20-21). Although Yoshida does not suggest verifying data (i.e., SA) transferred between a data processor and a network adapter card, one of ordinary skill

in any computer field that deals with data transfer between a data processor and a peripheral device would recognize from Yoshida reference that data transfer errors do happen when data is transferred between a processor and a peripheral device and that there is a need for data verification between those two components to protect the integrity of transferred data. Such teaching is general in principle and could be applied to any type of peripheral device and not just a hard disk drive. Therefore, it would have been obvious to apply the teachings of Yoshida to Anand.

Applicant argues that if the data verification techniques of Yoshida were applied to the system of Anand and all data transferred to the NIC was verified in the manner disclosed by Yoshida, the efficiency, speed and/or throughput of system of Anand would likely be decreased significantly; and because of that, the combination would not have been obvious (page 8, first full paragraph). First, cryptographic operations involving data encryption/decryption are expensive in terms of computational cost. Thus, by offloading those operations to a NIC, Anand's invention would greatly increase the overall computing efficiency of a computer system. In the other hand, Yoshida's data verification method involves only simple operations (i.e., calculating a checksum value and comparing two checksum values), which requires little computing resource. Therefore, the impact of implementing Yoshida data verification method on the efficiency and/or

throughput of Anand system would be minimal. Secondly, while the speed/throughput of a system is important, the correctness of the system's output/result is equally, if not even more, important. For security systems that handle sensitive data such as those in finance, banking, e-commerce, etc., correctness is something that would not be compromised by speed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 24-26, 28-31, 33-36, 38-41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand et al (6,370,599) in view of Yoshida (5,928,372).

Regarding claim 39, which are representative of claims 24, 29 and 34, Anand discloses a system comprising: a network adapter being capable of being coupled to an information handling apparatus (IHA) via a bus (fig. 1, elements 53, 21-23), said network adapter comprising an integrated circuit capable of receiving a security association (SA) generated by said IHA (col. 8, lines 21-35; figures 3-4 and corresponding text). Anand also discloses

that the network adapter receives the security association associated with a data packet to be encrypted (outgoing packet) or to be decrypted (incoming packet), encrypts or decrypts the data packet accordingly (col. 3, lines 47-60; col. 7, lines 55-64; col. 11, lines 1-6 and 24-44; col. 12, lines 15-19). Anand further discloses that the computer system including the network interface connects to a network infrastructure device (col. 6, line 65 – col. 7, line 6). Anand teaches transferring data from the IHA (i.e., the CPU) to the network adapter; however Anand does not teach verification of data transferred between the CPU and the network adapter, which is a peripheral device, and indicating the integrity of the received SA to the IHA. Yoshida teaches data verification in a data transfer system in which a host processor transfers data and a first integrity indicator generated by the host processor to a peripheral device (i.e., the hard disk unit) and the peripheral device generates a second integrity indicator, verifies that the received data is similar to the data sent by the host processor by comparing said first integrity indicator to said second integrity indicator, and indicating the integrity of the received data to the host processor (col. 1, line 60 – col. 2, line 20; figures 20-21 and corresponding text). Anand and Yoshida are analogous art because they are from a similar problem solving area, which is transferring data from a host processor to a peripheral device. It would have been obvious to one of ordinary skill in the art at the time the invention

was made to incorporate the Yoshida's teaching of data verification into the Anand system in order to insure the correctness of the reception data (col. 9, lines 47-54). Accordingly, the IHA generates and sends a first integrity indicator to the integrated circuit, the integrated circuit receives the first integrity indicator, generates a second integrity indicator based on said SA, verifies that said SA received by said integrated circuit is substantially similar to the SA generated by said IHA by comparing said first integrity indicator to said second integrity.

Anand does not explicitly disclose that the network adapter comprises an encoder (data encryption component) and a decoder (data decryption component); however, these components are inherent to Anand network adapter as lines 47-60 of column 3, lines 55-64 of column 7, and lines 24-44 of column 11 show that Anand network adapter encrypts outgoing data and decrypts incoming data using the received SA.

Regarding claims 25-26, 30-31, 35-36 and 40-41, Yoshida further discloses that the data checking integrity method used to generate the first and second integrity indicators is a cyclical redundancy checking computation method, a checksum computation method or a parity checking method (col. 10, lines 55-67).

Regarding claims 28, 33, 38 and 43, Yoshida does not explicitly disclose setting an integrity error indicator bit in a memory of the host

processor. However, this feature is deemed to be inherent to the Yoshida method as element 24 of figure 21 shows that the peripheral device provides the comparison result signal to the host processor. The Yoshida method would be inoperative if there were no register/memory on the host processor to store the comparison result signal.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dinh whose telephone number

is 571-272-3802. The examiner can normally be reached on Mon-Fri: 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MD

Minh Dinh
Examiner
Art Unit 2132

MD
1/27/07

GILBERTO BARRON JR
SUPERVISORY PATENT EXAMINER
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